4624 AWG Phaser

Features

- 4 channels of 1.25 GSPS 16-bit DAC
- 2 channels of 5 MSPS ADC
- Dual 0.3 GHz to 4.8 GHz IQ mixer w/ internal PLL
- 31.5 dB range digital step attenuator
- Xilinx Artix-7 FPGA core
- DDR3 SDRAM

Applications

- Driving acoustic optic deflectors (AOD) and acoustic optic modulators (AOM)
- Driving RF electrodes in ion traps
- Laser intensity servo

General Description

4624 AWG Phaser is an 8hp Sinara EEM, part of the ARTIQ/Sinara family. It adds versatile arbitrary wave generation (AWG) capabilities to carrier cards such as Kasli 2.0 and Kasli-SoC, with quadrature modulation compensation and interpolation features. It is available in two variants: Upconverter, which includes integrated RF upconversion, and Baseband, without it.

The Upconverter variant supplies two channels of digital-to-analog conversion (DAC), routed through dual IQ (Quadrature) mixers, with voltage-controlled oscillators for precise frequency generation and modulation. The Baseband variant supplies four channels of DAC directly. Both variants include two channels of analog-to-digital conversion (ADC) at 5 MSPS.

Multiple gateware variants exist for 4624 AWG Phaser, including MIQRO, available separately from QUARTIQ, which is capable of generating up to 16 dynamic tones.
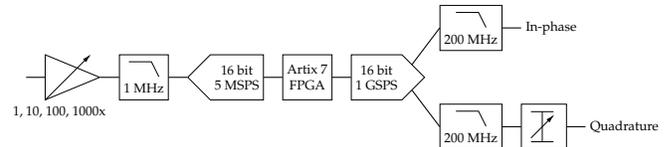

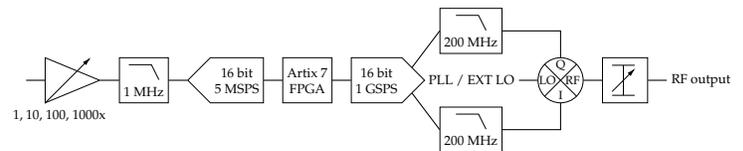Figure 1: Baseband Variant Block Diagram

Figure 2: Upconverter Variant Block Diagram

Figure 3: Phaser card

Figure 4: Phaser front panel

Source

4624 AWG Phaser, like all the Sinara hardware family, is open-source hardware, and design files (schematics, PCB layouts, BOMs) can be found in detail at the repository `https://github.com/sinara-hw/Phaser/`.

Specifications

Specifications are drawn up with reference to the Sinara wiki[1], Norman Krackow's thesis on the use of Phaser for short-time Fourier transform[2], and the datasheets of the DAC (DAC34H84[3]), ADC (LTC2323-16[4]), and IQ mixer (TRF372017[5]).

Table 1: Output Specifications

Parameter	Min.	Typ.	Max.	Unit	Conditions
DAC[3]					
Resolution		16		bits	
Sample rate		1.25		GSPS	
IQ modulator[5]					IQ mixer present on Upconverter variant only
LO frequency	0.3		4.8	GHz	
Third-order intercept point		26		dBm	750 MHz LO frequency
Carrier feedthrough		–43.5		dBm	750 MHz LO frequency
Sideband suppression		–46		dBc	750 MHz LO frequency
Output digital attenuation	-31.5		0	dB	Only In-phase outputs are attenuated on Baseband variant
Output power					
			1.61	dBm	10 MHz IF frequency, Baseband variant
			-1.36	dBm	10 MHz IF and 1 GHz LO frequency, Upconverter variant

[1] `https://github.com/sinara-hw/Phaser/wiki`
[2] `https://m-labs.hk/thesis_nkrackow.pdf`
[3] `https://www.ti.com/lit/ds/symlink/dac34h84.pdf`
[4] `https://www.analog.com/media/en/technical-documentation/data-sheets/232316fc.pdf`
[5] `https://www.ti.com/lit/ds/symlink/trf372017.pdf`

Table 2: Input Specifications

Parameter	Min.	Typ.	Max.	Unit	Conditions
ADC[4]					
Resolution		16		bits	
Sample rate		5		MSPS	
AFE input voltage	-11		11	V	1x gain, termination off*
	-1.1		1.1	V	10x gain
	-110		110	mV	100x gain
	-11		11	mV	1000x gain
External LO input					
Frequency	0.3		4.8	GHz	
Power			2	dBm	
DC input signal impedance		200		kΩ	Termination off
		50		Ω	Termination on

*With the 50Ω termination enabled, the input voltage magnitude must not exceed 5V.

Clock input may be supplied to 4624 AWG Phaser using either the internal MMCX connector or the external SMA connector in the front panel.

FPGA

4624 AWG Phaser features a XC7A100T Xilinx Artix-7 FPGA to to facilitate reconfigurable high-speed control of wave generation, sampling, and servo capabilities. Phaser was designed as a flexible hardware platform for many different signal generation schemes; multiple gateware configurations exist covering different use-cases, and more could be designed.

M-Labs normally provides 4624 AWG Phaser under the "classic" configuration, which hosts fixed interpolators and subsequent digital upconverters for two RF output channels. A notable alternative configuration is MIQRO, available separately from QUARTIQ.

Phaser I/O

The front panel of 4624 AWG Phaser features a total of five SMA connectors, individually labeled. Clock input is available over `EXT CLK IN`. The dual ADC channels are exposed respectively on `ADC IN0` and `ADC IN1`, with input termination by DIP switch (see below). Depending on configuration, the four DAC output channels are either exposed directly (Baseband variant) or fed in pairs to the quadrature upconverters (Upconverter variant).

In the Upconverter variant, outputs from the upconverters are passed through the 31.5 dB range step attenuator and exposed in the front panel at `RF0` and `RF1`.

Figure 5: Position of U.FL DAC outputs

In the Baseband variant, two of four channels, the in-phase or even outputs, are available on `RF0` and `RF1`. Respective odd outputs (in either variant) are exposed by labeled U.FL connectors at back of board.

LEDs

4624 AWG Phaser provides six user LEDs, which are located in the front panel and respectively marked `LD0` to `LD5`. These are directly accessible in ARTIQ gateware and can be used for testing or feedback.

Configuring Termination

The input termination must be configured by setting physical switches on the board. The termination switches are found at the middle left part of the card and are by-channel. Setting these switches to `on` adds a 50Ω termination between the differential input signals.
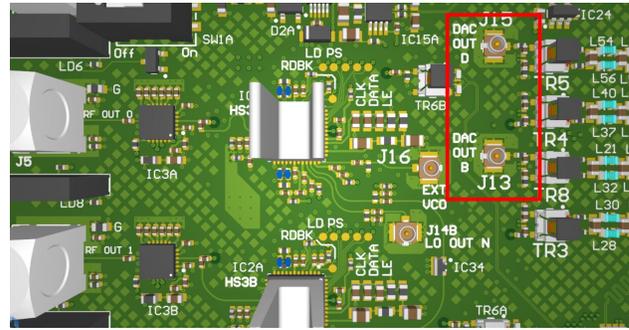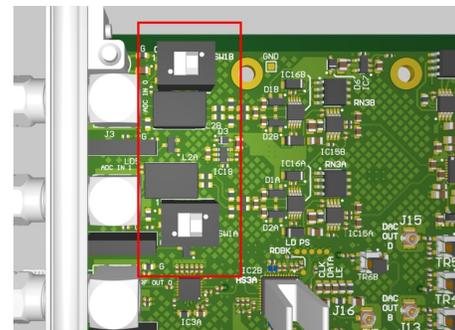
Figure 6: Position of switches

ARTIQ System Description Entry

ARTIQ/Sinara firmware/gateware is generated according to a JSON system description file, allowing gateware to be specific to and optimized for a certain system configuration.

4624 AWG Phaser should be entered in the `peripherals` list of the corresponding core device in the following format:

```
{
    "type": "phaser",
    "ports": [0]
}
```

Replace 0 with the EEM port number used on the core device. Any port can be used. On Phaser's side, two EEM ports are present, but only one is necessary; this should always be `EEM0`.

Example ARTIQ Code

The sections below demonstrate simple usage scenarios of extensions on the ARTIQ control system. These extensions make use of the resources of the 4624 AWG Phaser. They do not exhaustively demonstrate all the features of the ARTIQ system.

The full documentation for ARTIQ software and gateware, including guides for their use, is available at https://m-labs.hk/artiq/manual/. Please consult the manual for details and reference material of the functions and structures used here.

Phaser classic

Different Phaser gateware configurations should be treated differently in ARTIQ experiments. The Phaser driver exposes the superset of all functionality; features that are absent in the actual Phaser gateware configuration will not work and should not be accessed.

In the Phaser classic or base configuration, five oscillators are made available per channel. The following code sets the DUC (digital upconverter) and interpolator configurations, sets the channel attenuation, then sets a frequency and amplitude phase for all available oscillators.

```python
def set_phaser0_frequencies(self):
    self.core.break_realtime()
    self.phaser0.init()
    delay(1*ms)

    duc = 10*MHz
    osc = [i*1*MHz for i in range(5)]

    self.phaser0.channel[0].set_duc_frequency(duc)
    self.phaser0.channel[1].set_duc_frequency(-duc)

    for ch in range(2):
        self.phaser0.channel[ch].set_duc_cfg()
        self.phaser0.channel[ch].set_att(6*dB)
    self.phaser0.duc_stb()
    delay(1*ms)

    for i in range(len(osc)):
        self.phaser0.channel[0].oscillator[i].set_frequency(osc[i])
        self.phaser0.channel[0].oscillator[i].set_amplitude_phase(.2)
        self.phaser0.channel[1].oscillator[i].set_frequency(-osc[i])
        self.phaser0.channel[1].oscillator[i].set_amplitude_phase(.2)
        delay(1*ms)
```

Ordering Information

To order, please visit https://m-labs.hk and choose 4624 AWG Phaser in the ARTIQ/Sinara hardware selection tool. Cards can be ordered as part of a fully-featured ARTIQ/Sinara crate or standalone through the 'Spare cards' option. Otherwise, orders can also be made by writing directly to mailto:sales@m-labs.hk.