4624 / 4625 AWG Phaser

Features

- 4 channels of 1.25 GSPS 16-bit DAC
- 2 channels of 5 MSPS ADC
- Dual 0.3 GHz to 4.8 GHz IQ mixer w/ internal PLL
- 31.5 dB range digital step attenuator
- Xilinx Artix-7 FPGA core, DDR3 SDRAM

Applications

- Driving acoustic optic deflectors (AOD) and acoustic optic modulators (AOM)
- Driving RF electrodes in ion traps
- Laser intensity servo

General Description

4624/4625 AWG Phaser is an 8hp Sinara EEM, part of the ARTIQ/Sinara family. It adds versatile arbitrary wave generation (AWG) capabilities to carrier cards such as Kasli v2 and Kasli-SoC, with quadrature modulation compensation and interpolation features. It is available in two variants: 4625 Phaser Upconverter, which includes integrated RF upconversion, and 4624 Phaser Baseband, without it.

The 4625 Upconverter variant supplies two channels of digital-to-analog conversion (DAC), routed through dual IQ (Quadrature) mixers, with voltage-controlled oscillators for precise frequency generation and modulation. The 4624 Baseband variant supplies four channels of DAC directly. Both variants include two channels of analog-to-digital conversion (ADC) at 5 MSPS.

Multiple gateware variants exist for 4624/4625 AWG Phaser, including Phaser MTDDS (Multi-Tone DDS), which allows Phaser to act as a full DRTIO node with 2 IQ channels of up to 26 tones each.

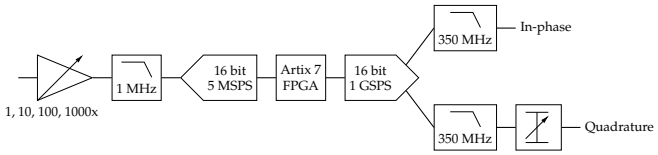

Figure 1: Baseband Variant Block Diagram

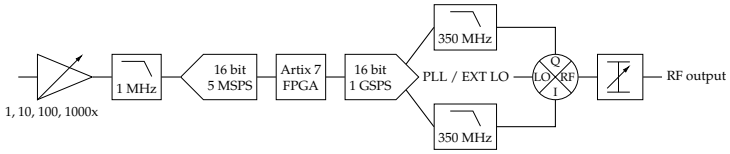

Figure 2: 4625 Upconverter Variant Block Diagram

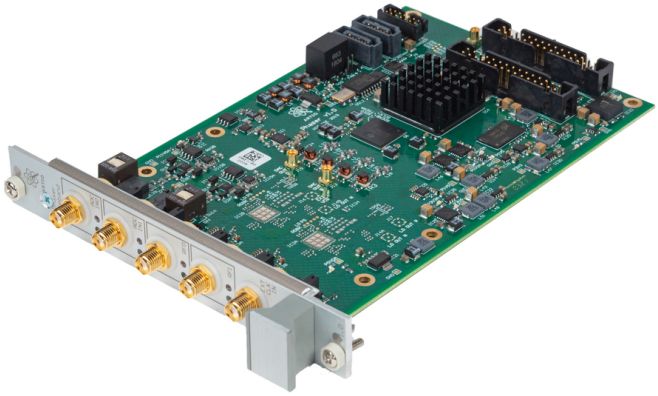

Figure 3: Phaser card

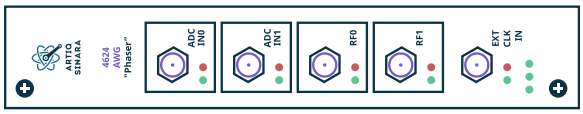

Figure 4: Phaser front panel (4hp)

Source

4624 AWG Phaser, like all the Sinara hardware family, is open-source hardware, and design files (schematics, PCB layouts, BOMs) can be found in detail at the repository https://github.com/sinara-hw/Phaser/.

Specifications

Specifications are drawn up with reference to the Sinara wiki[1], Norman Krackow's thesis on the use of Phaser for short-time Fourier transform[2], and the datasheets of the DAC (DAC34H84[3]), ADC (LTC2323-16[4]), and IQ mixer (TRF372017[5]).

Table 1: Output Specifications

Parameter	Min.	Typ.	Max.	Unit	Conditions
DAC[3]					
Resolution		16		bits	
Sample rate		1.25		GSPS	
IQ modulator[5]					IQ mixer present on 4625 Upconverter variant only
LO frequency	0.3		4.8	GHz	
Third-order intercept point		26		dBm	750 MHz LO frequency
Carrier feedthrough		–43.5		dBm	750 MHz LO frequency
Sideband suppression		–46		dBc	750 MHz LO frequency
Output digital attenuation	-31.5		0	dB	Only in-phase outputs are attenuated on Baseband variant
Output power					
			1.61	dBm	10 MHz IF frequency, 4624 Baseband variant
			-1.36	dBm	10 MHz IF and 1 GHz LO frequency, 4625 Upconverter variant

[1] https://github.com/sinara-hw/Phaser/wiki
[2] https://m-labs.hk/thesis_nkrackow.pdf
[3] https://www.ti.com/lit/ds/symlink/dac34h84.pdf
[4] https://www.analog.com/media/en/technical-documentation/data-sheets/232316fc.pdf
[5] https://www.ti.com/lit/ds/symlink/trf372017.pdf

Table 2: Input Specifications

Parameter	Min.	Typ.	Max.	Unit	Conditions
ADC[4]					
Resolution		16		bits	
Sample rate		5		MSPS	
AFE input voltage	-11		11	V	1x gain, termination off*
	-1.1		1.1	V	10x gain
	-110		110	mV	100x gain
	-11		11	mV	1000x gain
External LO input					
Frequency	0.3		4.8	GHz	
Power			2	dBm	
DC input signal impedance		200		kΩ	Termination off
		50		Ω	Termination on

*With the 50Ω termination enabled, the input voltage magnitude must not exceed 5V.

Clock input may be supplied to 4624/4625 AWG Phaser using either the internal MMCX connector or the external SMA connector in the front panel.

Note that by front panel dimensions alone, Phaser is a 4hp EEM card. Its classification as 8hp is a result of the additional space required by a fan, which causes the card to exceed 4hp width in total. However, if placed next to a short card like 2128 SMA-TTL, 4624/4625 AWG Phaser requires only 4hp of rack space.

FPGA

4624/4625 AWG Phaser features a XC7A100T Xilinx Artix-7 FPGA to to facilitate reconfigurable high-speed control of wave generation, sampling, and servo capabilities. Phaser was designed as a flexible hardware platform for many different signal generation schemes; multiple gateware configurations exist covering different use-cases, and more could be designed.

Configurations provided by M-Labs include Phaser MTDDS (Multi-Tone DDS), also known as Phaser DRTIO, which allows Phaser to act as a full DRTIO node with 2 IQ channels of up to 26 tones each, with configurable DDS bandwidth and direct interface access to ADC channels among other features. The older Phaser "classic" configuration, which acts as a standard peripheral hosting fixed interpolators and subsequent digital upconverters for two RF output channels, also remains available. A notable alternative is MIQRO, which can be obtained separately from QUARTIQ.

Phaser I/O

The front panel of 4624/4625 AWG Phaser features a total of five SMA connectors, individually labeled. Clock input is available over `EXT CLK IN`. The dual ADC channels are exposed respectively on `ADC IN0` and `ADC IN1`, with input termination by DIP switch (see below). Depending on configuration, the four DAC output channels are either exposed directly (4624 Baseband) or fed in pairs to the quadrature upconverters (4625 Upconverter).

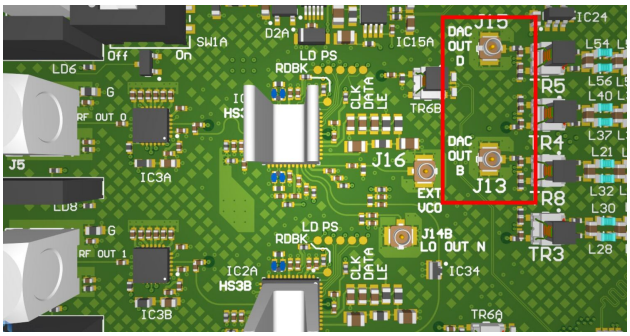

Figure 5: Position of Baseband in-phase outputs

With 4625 Upconverter, outputs from the upconverters are passed through the 31.5 dB range step attenuator and exposed in the front panel at `RF0` and `RF1`.

In the Baseband variant, quadrature outputs are passed through the 31.5 dB range step attenuator and exposed in the front panel at `RF0` and `RF1`, while the in-phase outputs are exposed by the U.FL connectors.

LEDs

4624/4625 AWG Phaser provides six user LEDs, which are located in the front panel and respectively marked `LD0` to `LD5`. These are directly accessible in ARTIQ gateware and can be used for testing or feedback.

Configuring Termination

The input termination must be configured by setting physical switches on the board. The termination switches are found at the middle left part of the card and are by-channel. Setting these switches to `on` adds a 50Ω termination between the differential input signals.

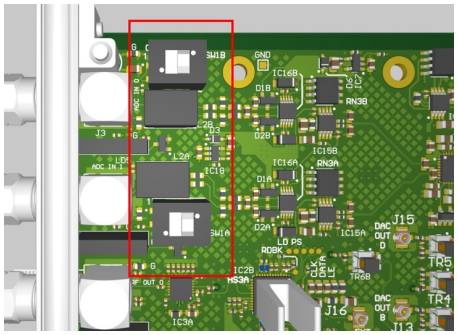

Figure 6: Position of switches

Anti-aliasing Filter

4624 AWG Phaser uses an anti-aliasing filter with a 350 MHz cutoff frequency. Older versions of the same card used a filter with a 200 MHz cutoff frequency; for more discussion of this design, see also the hardware source repository[6], [7]. Measurements below were performed on 4624 Phaser Baseband.

200 MHz filter (deprecated)

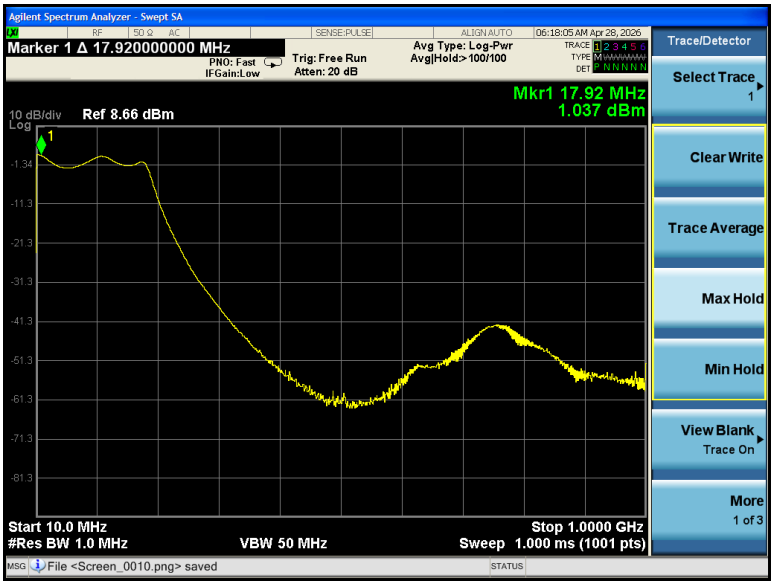

Figure 7: Frequency sweep, old AA filter

350 MHz filter (current)

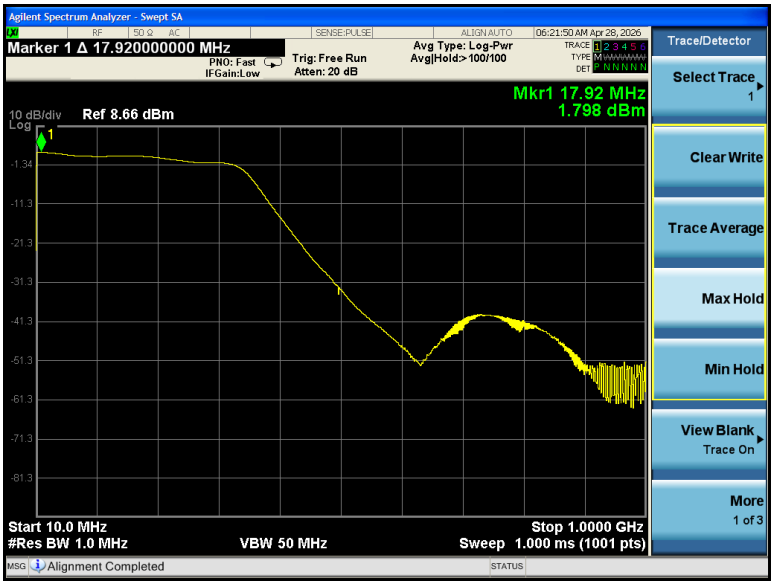

Figure 8: Frequency sweep, current AA filter

[6] https://github.com/sinara-hw/Phaser/issues/158
[7] https://github.com/sinara-hw/Phaser/issues/160

ARTIQ System Description Entry

ARTIQ/Sinara firmware/gateware is generated according to a JSON system description file, allowing gateware to be specific to and optimized for a certain system configuration.

4624/4625 AWG Phaser has multiple possible system description entries, depending on gateware on configuration. When flashed as MIQRO or Phaser Classic, 4624/4625 AWG Phaser should be entered in the `peripherals` list of the corresponding core device in the following format:

```
{
    "type": "phaser",
    "ports": [0]
}
```

Replace 0 with the EEM port number used on the core device. Any port can be used. 4624/4625 AWG Phaser itself provides two EEM ports, but only one is necessary; this should always be `EEM0`.

Phaser MTDDS

When flashed as Phaser MTDDS, 4624/4625 AWG Phaser should be entered in the `peripherals` list of the corresponding core device as follows:

```
{
    "type": "phaser_drtio",
    "gateware_variant": "mtdds",
    "hardware_variant": "upconverter", // or "baseband"
    "ports": [0],
    "tones": 26, // between 1 and 26
    "dds_bandwidth": 250e6, // or 500e6
    "drtio_destination": 4 // optional
}
```

Replace 0 with the EEM port number used on the core device. Any port can be used.

Since Phaser acts as a DRTIO satellite, the DRTIO type of the core device should be specified as master, not standalone, even if no other satellite cores are used. The `drtio_destination` field sets a DRTIO destination number for Phaser. This field is optional. If left unspecified, Phasers are automatically assigned a destination number, starting with #4 on Kasli v2, #5 on Kasli-SoC[8], counting up correspondingly for additional Phasers.

See the ARTIQ manual[9] for instructions on configuring a DRTIO routing table, if necessary for your layout (e.g. with a Phaser attached to a DRTIO satellite).

[8] i.e., in both cases, first available destination number after those associated with the core device's downstream SFP slots.
[9] https://m-labs.hk/artiq/manual/using_drtio_subkernels.html

Example ARTIQ Code

The sections below demonstrate simple usage scenarios of extensions on the ARTIQ control system. These extensions make use of the resources of the 4624/4625 AWG Phaser. They do not exhaustively demonstrate all the features of the ARTIQ system.

The full documentation for ARTIQ software and gateware, including guides for their use, is available at https://m-labs.hk/artiq/manual/. Please consult the manual for details and reference material of the functions and structures used here.

ARTIQ provides different Phaser drivers for different gateware configurations. The `phaser` driver exposes the superset of all functionality of Phaser as a peripheral, i.e. both Phaser "Classic" and MIQRO. The `phaser_drtio` exposes the functionality of Phaser as a DRTIO node, i.e. Phaser MTDDS. Features that belong to a configuration which is not flashed will not work and should not be accessed.

Phaser classic

In the Phaser classic configuration, five oscillators are made available per channel. The following code sets the DUC (digital upconverter) and interpolator configurations, sets the channel attenuation, then sets a frequency and amplitude phase for all available oscillators.

```
def set_phaser0_frequencies(self):
    self.core.break_realtime()
    self.phaser0.init()
    delay(1*ms)

    duc = 10*MHz
    osc = [i*1*MHz for i in range(5)]

    self.phaser0.channel[0].set_duc_frequency(duc)
    self.phaser0.channel[1].set_duc_frequency(-duc)

    for ch in range(2):
        self.phaser0.channel[ch].set_duc_cfg()
        self.phaser0.channel[ch].set_att(6*dB)
    self.phaser0.duc_stb()
    delay(1*ms)

    for i in range(len(osc)):
        self.phaser0.channel[0].oscillator[i].set_frequency(osc[i])
        self.phaser0.channel[0].oscillator[i].set_amplitude_phase(.2)
        self.phaser0.channel[1].oscillator[i].set_frequency(-osc[i])
        self.phaser0.channel[1].oscillator[i].set_amplitude_phase(.2)
        delay(1*ms)
```

Ordering Information

To order, please visit https://m-labs.hk and choose 4624/4625 AWG Phaser in the ARTIQ/Sinara hardware selection tool. Cards can be ordered as part of a fully-featured ARTIQ/Sinara crate or standalone through the 'Spare cards' option. Otherwise, orders can also be made by writing directly to mailto:sales@m-labs.hk.

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